

Form PTO-1449 (Substitute)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Attorney Docket Number ANTR-01016US0		Serial/Patent Number: 09/589,966	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use several sheets if necessary)</i>				DEC 27 2000 PATENT & TRADEMARK OFFICE U.S. DEPARTMENT OF COMMERCE			
				Applicant/Patent Owner Michael J. Demler			
				Filing/Issue Date June 8, 2000		Group Art Unit 2837	
PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
T.P.	1.	5,345,409	9/6/94	McGrath et al.	364	736	03/25/93
T.P.	2.	5,659,312	8/19/97	Sunter et al.	341	120	06/14/96
T.P.	3.	5,714,902	2/3/98	Comer	327	346	11/30/95
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Subclass	Trans- lation Yes No
OTHER DOCUMENTS (Include Author, Title, Date, Pertinent pages, etc.)							
Examiner <u>Thai Phan</u>				Date Considered <u>1/27/03</u>			
<p>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p> <p>*1 = Copy not submitted because it was submitted in prior application SN / _____, filed _____, 19 _____. *2 = Copy not submitted because it was submitted in prior application SN / _____, filed _____, 19 _____.</p>							



Sheet 1 of 1

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		Filing/Issue Date June 8, 2000		Group Art Unit 2837 2123			
U.S. PATENTS							
Examiner Initial		Patent Number	Issue Date	Inventor	Class	Subclass	Filing Date
T.P.		5,404,319	April 4, 1995	Smith et al.	364	578	02/11/93
OTHER DOCUMENTS (Include author (if any), title, publisher and place of publication, date and pertinent pages)							
T.P.	1.	Antao, B.A.A. and Brodersen, A.J., "ARCHGEN: Automated Synthesis of Analog Systems," <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , Vol. 3, No. 2, June 1995, pp. 231-244.					
T.P.	2.	Antao, B.A.A. and Brodersen, A.J., "Behavioral Stimulation for Analog System Design Verification," <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , Vol. 3, No. 3, September 1995, pp. 417-429.					
T.P.	3.	Antrim Design Systems, Inc., "The Characterization and Behavioral Model Generation of Analog Intellectual Property," <i>Antrim Design Systems White Paper</i> , May 1998, pp. 1-8, www.antrim.com.					
T.P.	4.	Borchers, C., "Symbolic Behavioral Model Generation of Nonlinear Analog Circuits, <i>IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing</i> , Vol. 45, No. 10, October 1998, pp. 1362-1371.					
T.P.	5.	Smith, J.T. and Brown, H.K., "Mixed-Signal Circuit Simulation System with Behavioral Modeling Capability," <i>IEEE Conference Record of Southcon/94</i> , March 1994, pp. 580-583.					
Examiner <u>Thai Phan</u>			Date Considered <u>01/27/03</u>				
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